a wordline plurality of wordlines wherein each of said plurality of wordlines is associated with a one of said plurality of rows in the array;

a plurality of bitlines wherein each of said plurality of bitlines is associated with one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with a one of said plurality of rows and a one of said plurality of columns in the array, each one of said plurality of nonvolatile memory transistors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of wordlines of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of bitlines of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory being couple to the source of each of said other ones of said plurality of nonvolatile memory transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors;

a plurality of source transistors wherein each one of said plurality of source transistors has a gate coupled to a one of said plurality of wordlines, a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation well in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.

24. An array of nonvolatile memory cells arranged in a plurality of rows and a plurality of columns comprising:

a substrate upon which said array is deposited;

a plurality of wordlines wherein each of said plurality of wordlines is associated with a one of said plurality of rows in the array;

a plurality of bitlines wherein each of said plurality of bitlines is associated with one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with a one of said plurality of rows and a one of said plurality of columns in the array, each one of said plurality of nonvolatile memory transistors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of wordlines of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of bitlines of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory being couple to the source of each of said other ones of said

plurality of nonvolatile memory transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors;

a plurality of source transistors wherein each one of said plurality of source transistors has a gate coupled to a one of said plurality of wordlines a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation wells in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.

37. An array of one-time programmable nonvolatile memory cells arranged in a plurality of rows and a plurality of columns comprising:

a substrate upon which said array is deposited;

a plurality of wordlines wherein each of said plurality of wordlines is associated with a one of said plurality of rows in the array;

a plurality of bitlines wherein each of said plurality of bitlines is associated with one of said plurality of columns in the array;

a plurality of nonvolatile memory transistors, each of said nonvolatile memory transistors associated with a one of said plurality of rows and a one of said plurality of columns in the array, each one of said plurality of nonvolatile memory

transistors having a source, a drain, a floating gate and a control gate, the control gate of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of wordlines of said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistor, the drain of each one of said plurality of nonvolatile memory transistors coupled to the one of said plurality of bitlines of said one of said plurality of columns associated with said one of said plurality of nonvolatile memory transistors, the source of each one of said plurality of nonvolatile memory being couple to the source of each of said other ones of said plurality of nonvolatile memory transistors in said one of said plurality of rows associated with said one of said plurality of nonvolatile memory transistors;

a plurality of source transistors wherein each one of said plurality of source transistors has a gate coupled to a one of said plurality of, a source coupled to a source potential line, and a drain coupled to the sources of each of said plurality of nonvolatile memory transistors associated with said one of said plurality of rows associated with said wordline coupled to said source of said one of said plurality of source transistors;

a plurality of isolation well in said substrate wherein a portion of said plurality of nonvolatile memory transistors associated with a byte of data are disposed in each of said plurality of isolation wells; and

a plurality of well selection transistors wherein each one of said plurality of well selection transistors is connected to a one of said plurality of isolation wells.